A HIGH DYNAMIC RANGE, DIGITALLY TUNED, Q-ENHANCED LC BANDPASS FILTER FOR CELLULAR/PCS RECEIVERS

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ABSTRACT

A fully-integrated, 850 MHz, 2-pole, bandpass filter with a 2 percent fractional bandwidth is reported. The filter provides digital control of center frequency and Q, and includes a companion on-chip oscillator suitable for master-slave tuning. Prototype measurements show a dynamic range of 75 dB when used in a system with a 1 MHz final IF bandwidth, and an oscillator phase noise of -105 dBc/Hz at 100 kHz offset.

1. INTRODUCTION

Q-enhancement of on-chip spiral inductors has been proposed as a means to realize narrow fractional bandwidth RF filters suitable for use in receiver front-end and first IF circuits [1] [2] [3] [4]. The basic technology has been shown to be theoretically viable for such applications [5], but to-date, reported implementations have realized only moderate dynamic range performance (e.g. 50 dB) and have not addressed manufacturability issues or the need for real-time tuning in practical high-order designs. The implementation reported here is a full fourth-order (2 pole) design operating at 850 MHz with a 2 percent (18 MHz) bandwidth. It achieves a 75 dB dynamic range when used in a cellular or PCS receiver with a nominal 1 MHz channel bandwidth and includes a companion oscillator for use in master-slave tuning.

2. CHIP ARCHITECTURE

The experimental chip architecture is shown in Figure 1. Three fully-differential, on-chip LC resonators are constructed around three 500 μm, 8-turn, center-tapped spiral inductors [6]. Two of the three resonators are identical and form the core of a coupled-resonator filter. The remaining resonator is configured to operate as an on-chip oscillator at a fixed 60 MHz offset from the filter passband. This offset prevents excessive magnetic coupling of the large amplitude oscillator signal into the filter and allows the oscillator to double as an LO for down-conversion to a 60 MHz IF, while fulfilling its primary role as a tuning reference in a master-slave filter tuning architecture.

To yield a fourth-order response with the desired bandwidth, the filter inductors are magnetically coupled through suitable placement on the die. With ideal inductors, magnetic coupling between filter resonators would result in an induced voltage in one inductor which is in phase quadrature with the current in the opposite inductor, and therefore in-phase with the opposite resonator's voltage waveform. These phase relationships are necessary for a flat passband response. However, with on-chip spiral inductors, inductor currents and voltages are not in quadrature due to the large series resistances present, and significant passband asymmetries result [3]. A coupling neutralization circuit is placed between the two resonators in this design to cancel the undesired effects of the in-phase component of the inductor's I/V relationship. Digital control allows a simple one-time trim of passband ripple to better than 2 dB. Input-output transconductors provide buffering of the resonator circuits to external test equipment used in the prototype chip evaluation. Internal dummy transconductors shown in Figure 1 guarantee matching between resonators, simplifying tuning.

Filter and oscillator frequencies are set through 5-bit digital control words. Use of digital tuning allows high-Q tuning capacitors to be implemented, making resonator starting quality factor (before Q enhancement) primarily dependent on inductor Q. This maximization of starting Q is essential to achieving good dynamic range at acceptable power dissipation [5], and minimizes frequency drift [2]. Within each LC resonator, approximately 80 percent of the total C value originates from the inductor's turn-to-substrate capacitance, with the remaining C contributed by connected I/O buffers, Q tuning cells, and frequency tuning cells. Thus, resonator frequency is largely determined by ca-

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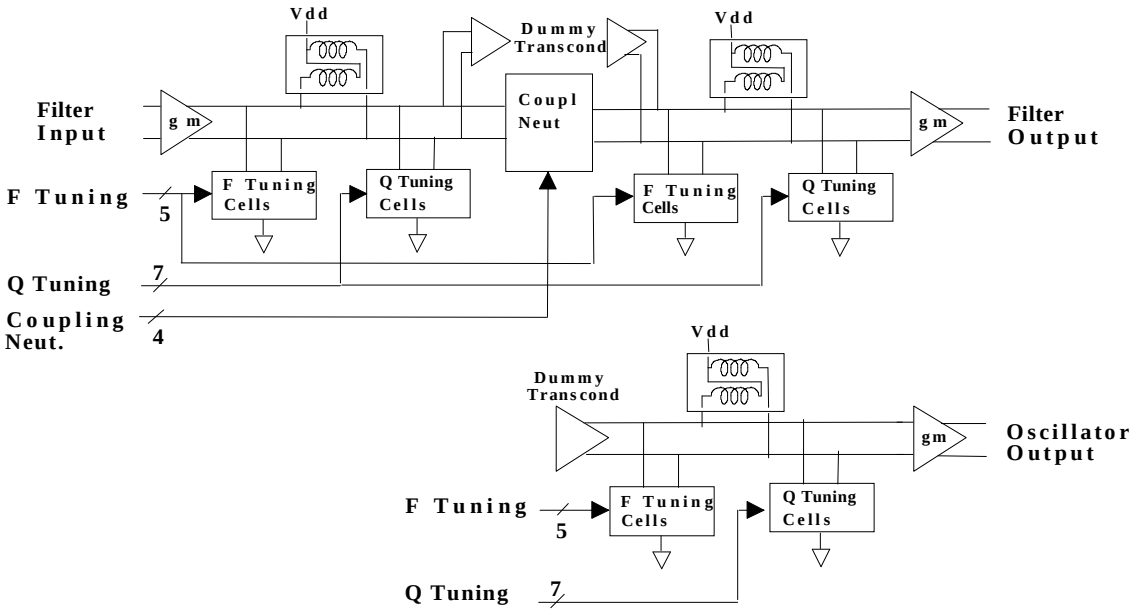

Figure 1. Chip Architecture.

pacitance within the inductor, allowing the tuning range to be relatively small in a process with tight oxide thickness tolerances. The prototype design provides a range of 60 MHz with a resolution of approximately 1.8 MHz (10 percent of the nominal filter bandwidth).

Tuning of filter Q is performed through a 7-bit digital control word, yielding the necessary range to compensate for variations in filter starting Q while providing a resolution of 15 percent of the nominal enhanced Q of 70. This Q resolution maps to a resolution of better than 20 percent in filter bandwidth.

As shown in Figure 1, identical controls are present in the companion oscillator circuit so that master-slave tuning can be implemented. Tuning can be accomplished by sensing the oscillator's amplitude and frequency, and constructing a suitable control loop to provide appropriate frequency and Q adjustments using a host system's microprocessor as described in [7].

3. FREQUENCY AND Q TUNING CIRCUITS

The circuit used for Q tuning is shown in Figure 2. The circuit implements a negative resistance used to offset losses within the resonators, raising the effective resonator Q. The core circuit consists of cross-coupled transconductor M1, M2 which provides the negative resistance function, switch M3 to enable or disable the circuit, and pullup M4 to guarantee that when disabled, the circuit remains off in the presence of large signal swings on the inductor. Transistors M5, M6 are used in the LSBs to decrease the effective transconductances below that possible with minimum geometry FETs. The MSB is implemented with 16 copies of the circuit, with transistors M5 and M6 deleted. Lesser significant bits are composed of 8, 4, 2, and 1 copy with M5, M6 deleted, while the two least significant bits use a single copy with M5, M6 included.

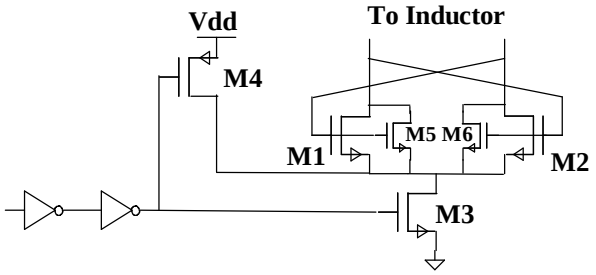

Figure 2. Q tuning cell.

Frequency tuning is performed by switching grounded capacitors in and out of the resonator circuits using suitable arrays of the core circuit of Figure 3. Metal-metal capacitors connected to the inductor are switched to ground on demand

through M1 and M2 which are sized to provide good capacitor Q when on. When M1, M2 are off, minimum geometry FETs M3 and M4 pull the drain of the larger M1, M2 transistors to Vdd - Vth, reducing M1, M2 parasitic capacitance and improving linearity. On-off capacitance ratio for the complete circuit is approximately 2:1 and the calculated quality factor of the capacitances is approximately 20 when on and 10 when off. This capacitor Q is found to have negligable effect on the resonator's starting Q when the relatively small fraction of total resonator capacitance contributed by the tuning circuits is taken into account.

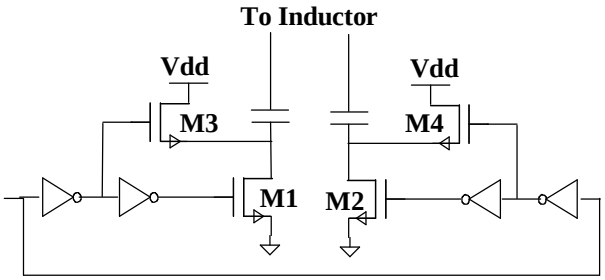

Figure 3. Frequency tuning cell.

4. MEASURED RESULTS

The filter and oscillator circuits described have been implemented in a standard 0.8 μm 1-poly, 3-metal, CMOS process. A photograph of the chip layout appears in Figure 4. The filter resonators are located in the upper half of the die while the associated oscillator is positioned at the lower right. The additional inductor in the lower left is part of a test structure for measuring the inductor performance.

The filter transfer characteristic S21 measured with external 4:1 impedance baluns is shown in Figure 5. Passband ripple was decreased from a starting value of 8 dB to the level shown using the chip's in-phase coupling neutralization controls. The two curves shown represent the two best neutralization settings. The residual 2 dB ripple could be reduced further with finer resolution controls. The desired 2 percent fractional bandwidth was achieved through appropriate setting of the Q controls and filter dynamic range was then measured as the ratio of the 1 dB compression output power (-18 dBm) to noise output power of -93 dBm measured in a 1 MHz resolution bandwidth, yielding 75 dB at a power dissipation of 208 mW. While this power consumption currently restricts applications to base/mobile systems, doubling inductor Q (from the current value of 3 to a modest value of 6) could allow this power consumption to be cut by four without sacrifices in dynamic range [5].

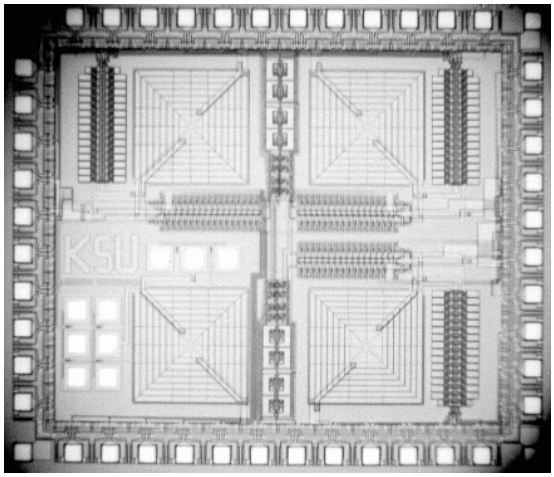

Figure 4. Die photograph.

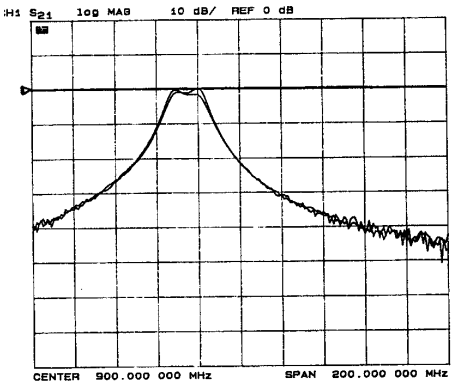

Figure 5. Measured filter response. 900 MHz center, 20 MHz/div.

The phase noise spectrum of the oscillator circuit is shown in Figure 6. Phase noise performance is -85 dBc/Hz at 10 kHz offset and -105 dBc/Hz at 100 KHz offset. The measured offset of oscillator frequency from filter passband center was 62 MHz and feedthrough from the oscillator into the filter was 20 dB below 1 dB compression in the second (output) resonator. Additional performance measurements are summarized in table 1.

5. CONCLUSIONS

The prototype design described in this paper achieves performance exceeding that of previous

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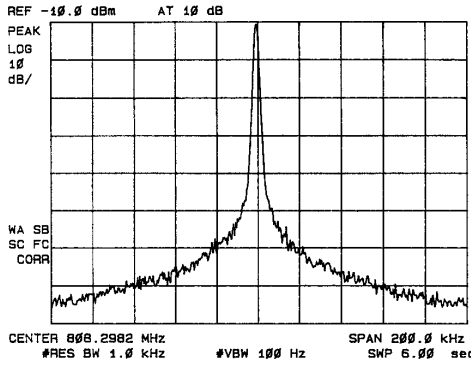

Figure 6. Measured oscillator noise. 1 kHz RBW, 20 kHz/div.

Table 1. Measured Performance

Parameter	Value
Transfer function type	2-pole coupled resonator
Center frequency	
Nominal	840 MHz
Min/max	816 MHz / 875 MHz
Open loop frequency drift	-250 ppm / °C
3 dB bandwidth	18 MHz
Midband gain	0 dB
Passband ripple	< 2 dB
Ultimate rejection	> 50 dB
Input 1 dB compression (in-band)	-18 dBm
Input referenced noise floor	
1 MHz final IF bandwidth	-93 dBm
30 kHz final IF bandwidth	-108 dBm
1 dB compression dynamic range	
1 MHz final IF bandwidth	75 dB
30 kHz final IF bandwidth	90 dB
Input third order intercept	
In-band	-10 dBm
40 MHz offset from center	+15 dBm
80 MHz offset from center	+28 dBm
Oscillator offset from filter	62 MHz
Oscillator phase noise	
10 kHz offset	-85 dBc/Hz
100 kHz offset	-105 dBc/Hz
Supply voltage	2.7 - 3.0 V
Supply current (at 2.7 V)	
Filter only	77 mA
Filter plus oscillator	114 mA
Die area (excluding pads)	2 mm^2

designs and implements all filter and oscillator circuits needed for achieving a practical fourth-order response. The technology provides a foundation for implementing high dynamic range, fully integrated receivers in cellular and PCS applications. Future reductions in power consumption through modest improvements in inductor Q could allow the technology to work in portable as well as base/mobile systems.

6. ACKNOWLEDGMENTS

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REFERENCES

[1] R.A. Duncan, K.W. Martin, and A.S. Sedra, "A Q-Enhanced Active-RLC Bandpass Filter," IEEE Int. Symp. on Circuits and Systems, 1993 pp. 1416-1419.

[2] Pipilos, Y.P. Tsividis, J. Fenk, and Y. Papananos, "A Si 1.8 GHz RLC Filter with Tunable Center frequency and Quality Factor," IEEE J. Solid-State Circuits, pp. 1517 - 1525, Oct. 1996.

[3] W.B. Kuhn, F.W. Stephenson, and A. Elshabini-Riad, "A 200 MHz CMOS Q-Enhanced LC Bandpass Filter," IEEE J. Solid-State Circuits, pp. 1112 - 1122, August 1996.

[4] C.-Y. Wu, and S.-Y. Hsiao, "The Design of a 3-V 900-MHz CMOS Bandpass Amplifier," IEEE J. Solid-State Circuits, pp. 159-167, Feb. 1997.

[5] W.B. Kuhn, F.W. Stephenson, and A. Elshabini-Riad, "Dynamic Range of High-Q OTA-C and Enhanced-Q LC RF Bandpass Filters," pp. 767-771, IEEE Midwest Symp. on Circuits and Systems, 1994.

[6] W. B. Kuhn, A. Elshabini-Riad, and F. W. Stephenson, "Centre-tapped Spiral Inductors for Monolithic Bandpass Filters," Electron. Lett., vol. 31, no. 8, pp. 625-626, 13 April 1995.

[7] W. B. Kuhn, *Design of Integrated, Low-Power, Radio Receivers in BiCMOS Technologies*, Ph.D. Dissertation, Bradley Department of Electrical Engineering, Virginia Polytechnic Institute and State University, Blacksburg, Virginia, December 1995.